REMARKS

Applicant respectfully requests favorable reconsideration of this application for the reasons presented below.

Claims 1-3, 5-21, 23-33 and 36 are the only claims currently pending in this application.

Applicant respectfully refers to the Office Action mailed December 5, 2005.

The Office Action recites a rejection of claims 1-3, 5-21, 23-33 and 36 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,848,619 ("*Leydier*"). Office Action at pp. 3-12.

Applicant respectfully traverses all of these rejections. The claims are amended for matters of form, for reasons not related to the rejections. Applicant references these now-pending claims in this response, but the amendments are not a waiver of Applicant's traversal, and do not constitute any disclaimer of claim scope or claimable subject matter. The amendments respectfully submits that properly interpreting these claims, or the examined claims, to have their broadest reasonable meaning, and then comparing the properly interpreted claims to the prior art of record, shows that all of claims stand in condition for allowance.

Applicant's claim 1 includes, among other elements, "a processor; a charge storage device coupled to the processor; and

> a *current source* for supplying the processor with
> *substantially constant operating current* at a level switchable
> among multiple *nonzero current levels*, and adapted to switch
> the level of the output operating current independently of an
> instantaneous power demand of the processor by switching,

on at least one of a periodic and an aperiodic basis, among
the multiple *nonzero current levels*

Claim 1, currently amended, at lines 4-9.

Illustrative support for the above-quoted claim 1 recitation is shown at, for example, Applicant's specification, page 3, lines 5-27, and at Applicant's Fig. 1. Referring to Applicant's Fig. 1, the depicted example includes a current source 12 that supplies the processor 11 with current Icc, and the current Icc is substantially constant at any of multiple, for example, two different nonzero levels. Specification at p. 3, lines 5-7.

Applicant respectfully submits that *Leydier* discloses *nothing* within the broadest reasonable meaning of the claim 1 language quoted above.

Leydier instead discloses an ON-OFF voltage source connecting to a load formed by capacitor CAP in parallel with a processor "uCE" and processor "uCL." The ON-OFF voltage source consists of the supply rail Vcc connecting to an ON-OFF switch "COM."

Applicant respectfully submits three facts, each of which standing alone establishes that *Leydier*'s structure *cannot* meet the claim 1 language.

The first fact is that *Leydier*'s ON-OFF switched supply is *not* a structure that falls within the broadest reasonable meaning of "a controllable *current* source." It is a *voltage* supply. Applicant respectfully submits a voltage supply is not within the broadest reasonable meaning of a current source.

The second of the three facts is that *Leydier's* voltage supply COM switch's output current is an exponential RC decay. *See Leydier* at Figs. 10A, 10B. Exponential rise-decay is not a "substantially constant" value. *Leydier* therefore does not disclose a supply outputting *any* constant output signal, much less a constant current, much less a constant current at multiple non-zero values. *Leydier's* OFF-ON COM voltage supply switch instead outputs, based on simple RC equations, a series of exponential rise-decay waveforms. *See Leydier* at Figs. 10B, 10C.

The third fact is that *Leydier's* voltage supply is an *ON-OFF* switched *voltage* supply. An ON-OFF switched voltage supply has *two* constant values, these are: (i) *zero*, and (ii) a given voltage. This is clear from *Leydier's* Figs. 10A, 10B; when its COM switch opens, the current from *Leydier's* COM voltage supply switch is necessarily *zero*. Zero, however, is *not* a "non-zero" value. Therefore, *Leydier's* ON-OFF voltage supply has only *one* non-zero constant value, which is its one given voltage. Applicant respectfully submits that the single non-zero value output from *Leydier' voltage* supply, in addition to not being a constant current, does *not* embody a structure that switches between *multiple non-zero*, constant current levels.

Applicant respectfully submits that each of three facts presented above, establishes that a fair and objective reading of *Leydier* shows that *Leydier* lacks subject matter meeting the broadest reasonable meaning of "a current …substantially constant current …at multiple different nonzero current levels."

Leydier therefore *cannot* anticipate Applicant's claim 1, or any of its dependent claims 2, 3, or 5-19.

Claim 20 is a method claim having subject matter substantially similar to claim 1 and, therefore, for at least the reasons Applicant presents for claim 1, *Leydier* cannot anticipate claim 20, or any of its dependent claims 21, 23-33 or 36.

With further respect to claim 3, the Office Action's position is that *Leydier* at col. 6, line 56, to col. 7, line 13; and at col. 8, lines 7-17, discloses "the current source ...switch[ing] between two different nonzero current levels." Office Action, at p. 3. The Office Action states a similar position on claim 21. *Id.*, at p. 8.

Applicant respectfully responds that the Office Action's position is in error. Applicant's claim 3 depends from claim 1, and claim 21 depends from claim 20. Claims 1 and 20 recite a *current source providing current to the processor*.

The cited sections of *Leydier*, in contrast, describe a technology for *the internal logic gates of the data processor itself*.

Applicant submits that interpreting Applicant's claim 1 and 20 recital of "a current source for supplying" current *to* a processor to encompass *an internal logic gate* of the processor requires misinterpreting the recited language far beyond its broadest reasonable meaning.

Applicant further submits that the cited sections of *Leydier* have nothing to do with the subject matter of Applicant's invention. The cited sections of *Leydier* describe a purportedly inventive structure and operation of the logic gate that, when summed over the N logic gates (*see Leydier* at col. 7, line 5), the total

consumption of energy is proportional to a supply voltage. This is *not* subject matter within the broadest reasonable meaning of the claim 3 and 21 language.

With further respect to claims 5 and 23, the Office Action's position is that *Leydier* at col. 6, line 56, through col. 7, line 13; and *Leydier* at col. 8, lines 7-17, teaches that "the interval between switching current levels is determined by an average power demand of the processor." *Id.*, at pp. 4, 8.

Applicant respectfully responds that the Office Action's position is in error; it departs from *Leydier's* disclosure, and/or it is not consistent with the broadest reasonable meaning of the claim 5 and 23 language. First, as Applicant submits above, *Leydier* lacks the base claim 1 and 20 current source. Second, the cited sections of *Leydier* describe the "SMC" gate technology, and how the energy consumed *by a particular logic gate* does not, purportedly, exhibit information indicative of the logical operands. See *Leydier*, at col. 8, lines 54-67. This has *nothing* to so with the subject matter of claims 5 and 23.

With further respect to claims 6 and 24, the Office Action's position is that *Leydier* at col. 8, lines 54-67; and at col. 10, lines 19-21, discloses a second current source adapted to provide a noise current. *Id.*, at pp. 4, 8-9.

Applicant respectfully responds that the Office Action's positions on claims 6 and 24 are in error.

Claims 6 and 24 recite a second current source for supplying the processor. Applicant refers to Applicant's Fig. 1, showing example support with current supply 13 as one illustrative structure within the broadest reasonable meaning of claims 6

and 24. *Leydier*, in contrast, discloses no structure within the broadest reasonable

meaning of claims 6 and 24. *Leydier* at col. 8, lines 54-67, instead discusses the

current for the COM switch with respect to time. *Leydier* at col. 10, lines 19-21

discusses a pulse generator for controlling the COM switch. None of this embodies,

or suggests toward, any subject matter that is within the broadest reasonable

meaning of the claim 6 and 24 "second current source."

With further respect to claim 7, the Office Action takes the position that

Leydier's Abstract; and *Leydier* at col. 2. lines 27-60; and col. 4, lines 47-57, discloses

a control means adapted to maintain the supply voltage to the processor between an

upper voltage limit and a lower voltage limit. *Id.*, at p. 4.

Applicant respectfully responds that the Office Action's position on claim 7 is

in error. The claim 7 "control means" is a means-plus-function element under 35

U.S.C. § 112, ¶ 6. Applicant's disclosed structure for performing the function is a

control 10 for the current source 12 feeding the capacitor C. Referring to

Applicant's Fig. 3, this structure exploits the voltage across a capacitor being the

integral, with respect to time, of the current through the capacitor. The result of

the arrangement recited by claim 7is the Fig. 3 saw-tooth voltage ranging between

the upper and lower value.

The cited sections of *Leydier*, in contrast, describe controlling its COM switch

to its Vcc rail based on a single threshold value. This disclosed function is not with

the broadest reasonable meaning of the claim 7 "control means" function, and this

disclosed structure is not equivalent to Applicant's disclosed structure within 35 U.S.C. § 112, ¶ 6.

Leydier, for similar reasons, lacks the various subject matters recited by Applicant's claims 8, 9, 25 and 26.

With respect to Applicant's claim 10, the Office Action's position is that *Leydier* at col. 2, lines 28-60; and at col. 4, lines 2025, discloses the claimed "timer for determining a time period taken." Office Action at p. 5.

Applicant respectfully responds that the Office Action's position on claim 10 is in error.

Claim 10 recites a "timer." The cited sections of *Leydier* describe controlling the frequency of the COM switch clock based on the voltage across the processor. Applicant respectfully submits this is not subject matter within the broadest reasonable meaning of the word "timer" as it appears in claim 10.

With respect to Applicant's claims 11-16, 28-31, and 36, the Office Action's position is that *Leydier*, at the various sections cited by the Examiner, discloses the subject matter of each of these claims. Office Action at pp. 5-7 and 10-11.

Applicant respectfully responds that the Office Action's positions on these claims are in error. All are inconsistent with the broadest reasonable meaning of the claim language, and/or lack support in *Leydier*'s disclosure.

Applicant submits, first, that all of claims 11-16, 28-31, and 36 recite *controlling a current between a first and a second current level*. *Leydier*, in contrast,

discloses nothing for supplying a *current level* to a processor, and much less controlling the level of a current to a processor.

Applicant submits, second, that all of these claims recite a *timer*, or determining a time for the processor voltage to move between limits. *Leydier* discloses *nothing* within the broadest reasonable meaning of a timer structure, or an act of timing.

Applicant submits, third, that all of these claims recite a timer, for determining a time for the processor voltage to move between *an upper and a lower limit*. *Leydier*, in contrast, discloses controlling the COM switch to the voltage rail Vcc based on a *single* threshold value.

With respect to claims 17 and 33, the Office Action's position is that *Leydier*, at col. 6, lines 19-25 and at Fig. 8, discloses a processor having an internal clock, the frequency of which is dependent upon the supply voltage to the processor. Office Action at pp. 5-7 and 10-11.

Applicant respectfully responds that the Office Action's positions on claims 17 and 33 are in error.

More particularly, *Leydier* at col. 6, lines 19-25 discusses variation in the current through a logic gate with respect to changes in the voltage of the logical operands. This has nothing to do with the recital of claims 17 or 33. The cited sections of *Leydier* do not disclose or suggest subject matter that is within the broadest reasonable meaning of claims 17 or 33.

CONCLUSION

In view of the remarks above, Applicant believes that each of the rejections/objections has been overcome and the application is in condition for allowance. In the event that the fees submitted prove to be insufficient in connection with the filing of this paper, please charge our Deposit Account Number 50-0578 and please credit any excess fees to such Deposit Account. Should there be any remaining issues that could be readily addressed over the telephone; the Examiner is asked to contact the agent overseeing the application file, David A. Cordeiro, of NXP Corporation at (408) 474-9075.

Respectfully submitted,
KRAMER & AMADO, P.C.

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